查询NE5209供应商

DATA SHEET

NE/SA5209
Wideband variable gain amplifier

Product specification

1990 Aug 20

RF Communications Handbook

PHILIPS

Wideband variable gain amplifier NE/SA5209

DESCRIPTION

The NE5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

PIN CONFIGURATION

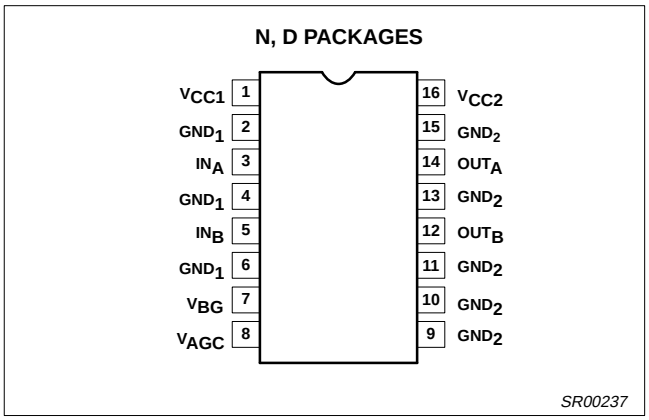


Figure 1. Pin Configuration

FEATURES

- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5209D	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5209N	SOT28-4
16-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5209D	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5209N	SOT28-4

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	38	43	48	mA
		Over temperature[1]	30		55	
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	17	19	21	dB
		Over temperature[1]	16		22	
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	23	25	27	dB
		Over temperature[1]	22		28	
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.9	1.2	1.5	kΩ
		Over temperature[1]	0.8		1.7	
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	40	60	75	Ω
		Over temperature[1]	35		90	
V_{OS}	Output offset voltage (output referred)			±20	±100	mV
		Over temperature[1]			±250	
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
		Over temperature[1]	1.4		2.6	
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
		Over temperature[1]	1.7		3.1	
PSRR	Output offset supply rejection ratio (output referred)		20	45		dB
		Over temperature[1]	15			
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
		Over temperature[1]	1.1		1.55	

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
R_{BG}	Bandgap loading	Over temperature[1]	2	10		kΩ
V_{AGC}	AGC DC control voltage range	Over temperature[1]		0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		-0.7	-6	µA
		Over temperature[1]			-10	

NOTES:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth		600	850		MHz
		Over temperature[1]	500			
GF	Gain flatness	DC - 500MHz		±0.4		dB
		Over temperature[1]		±0.6		
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[2]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[2]	R_L = 50Ω		400		mV_{P-P}
		R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		nV/√Hz
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.
2. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5209 APPLICATIONS

The NE5209 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 2. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5209 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5209 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5209 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5209 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5209. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5209 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5209 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5209 is shown in Figure 3. Three NE5209s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5209s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5209s will give a dynamic range in excess of 60dB.

The NE5209 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

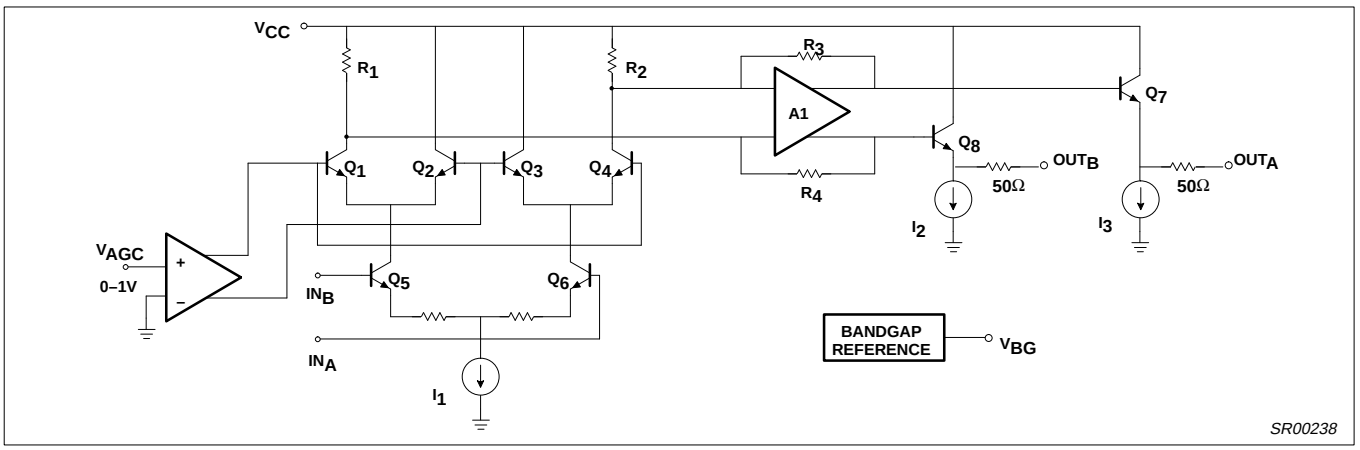


Figure 2. Equivalent Schematic of the VGA

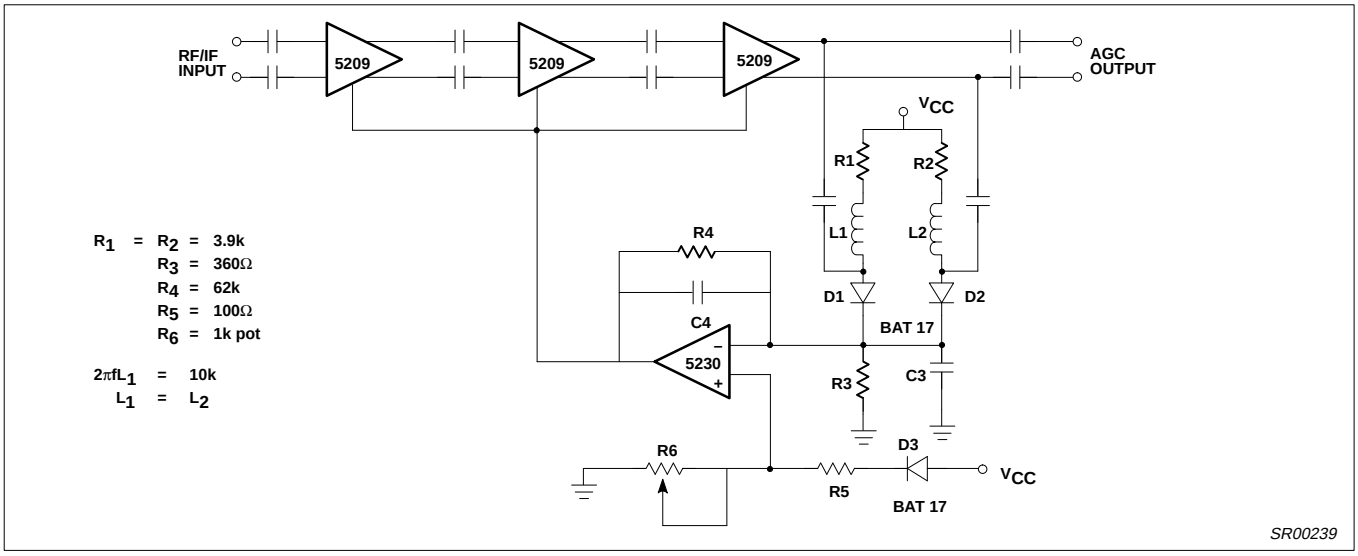


Figure 3. AGC Configuration Using Cascaded NE5209s

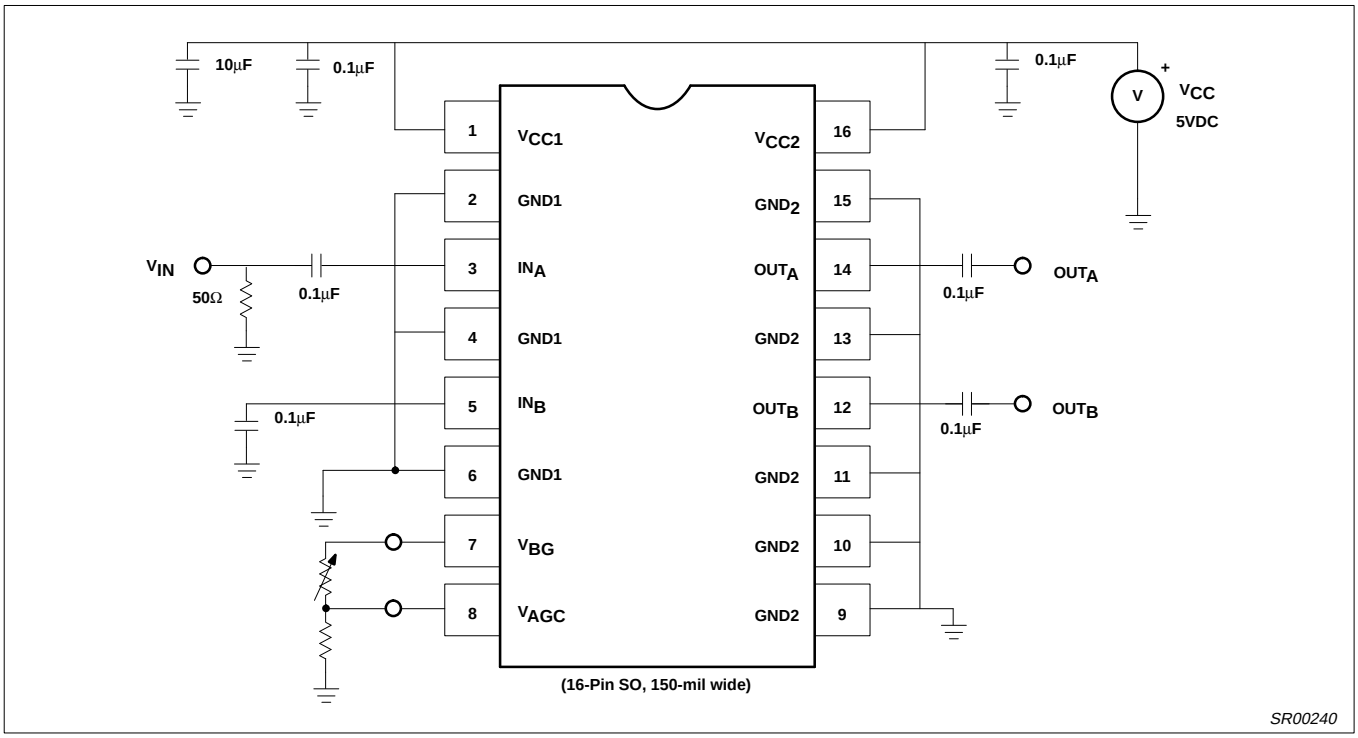


Figure 4. VGA AC Evaluation Board

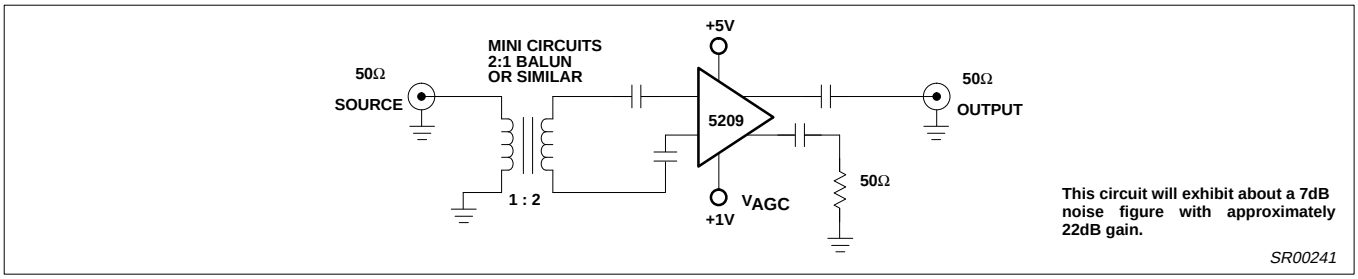
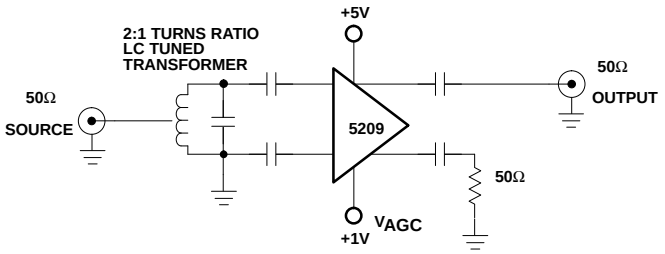
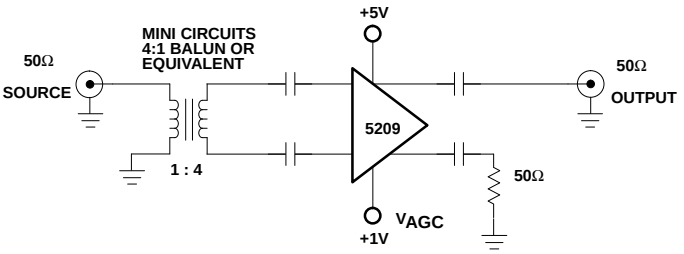


Figure 5. Broadband Noise Optimization



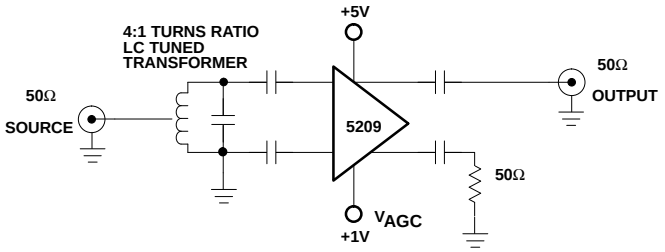
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 6. Narrowband Noise Optimization



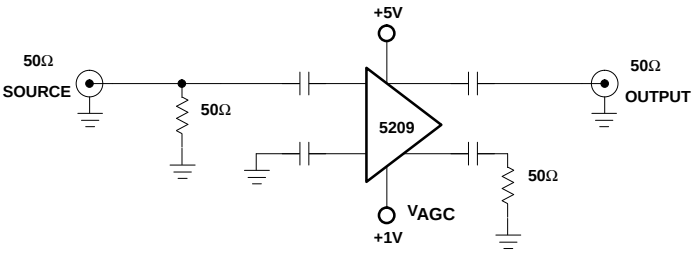
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 7. Broadband Gain Optimization



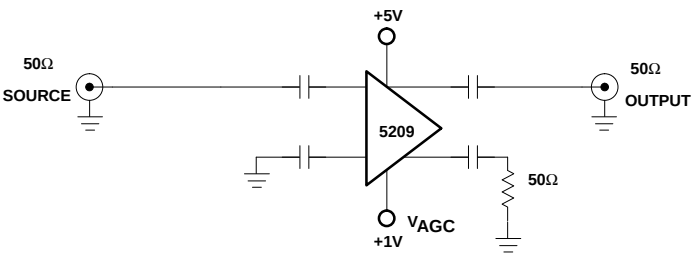
This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 8. Narrowband Gain Optimization



The noise figure of this configuration will be approximately 15dB.

Figure 9. Simple Amplifier Configuration



With the 50Ω source left unterminated, the noise figure is 9dB.

Figure 10. Unterminated Configuration

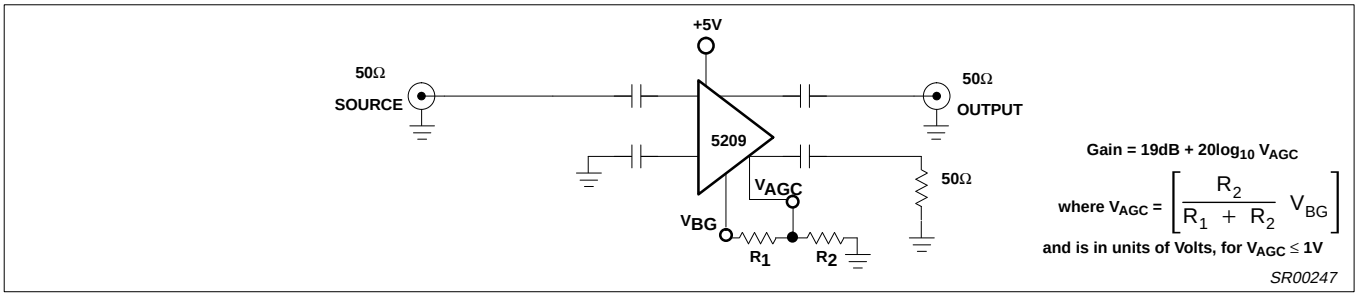


Figure 11. User-Programmable Fixed Gain Block

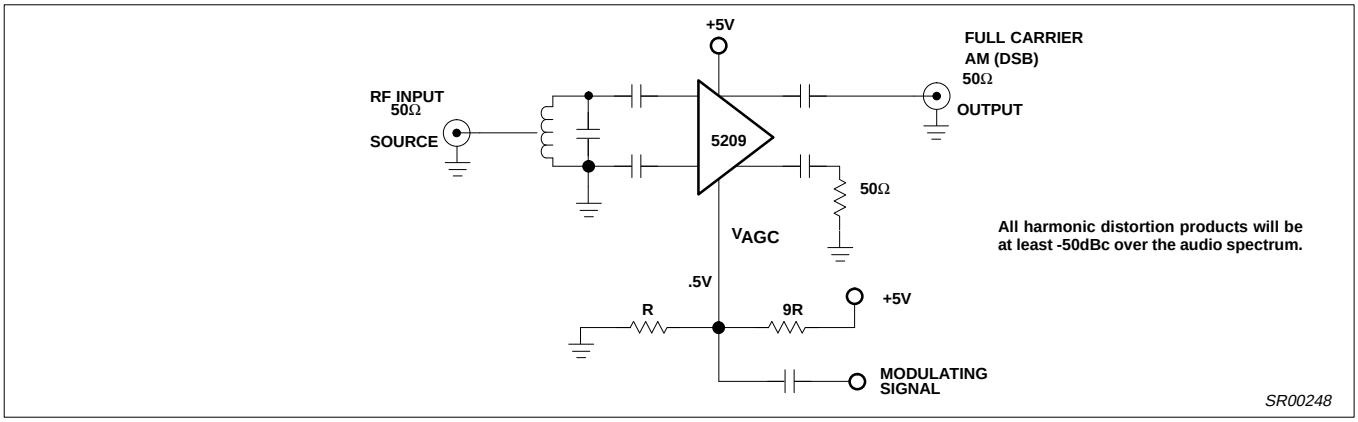


Figure 12. AM Modulator

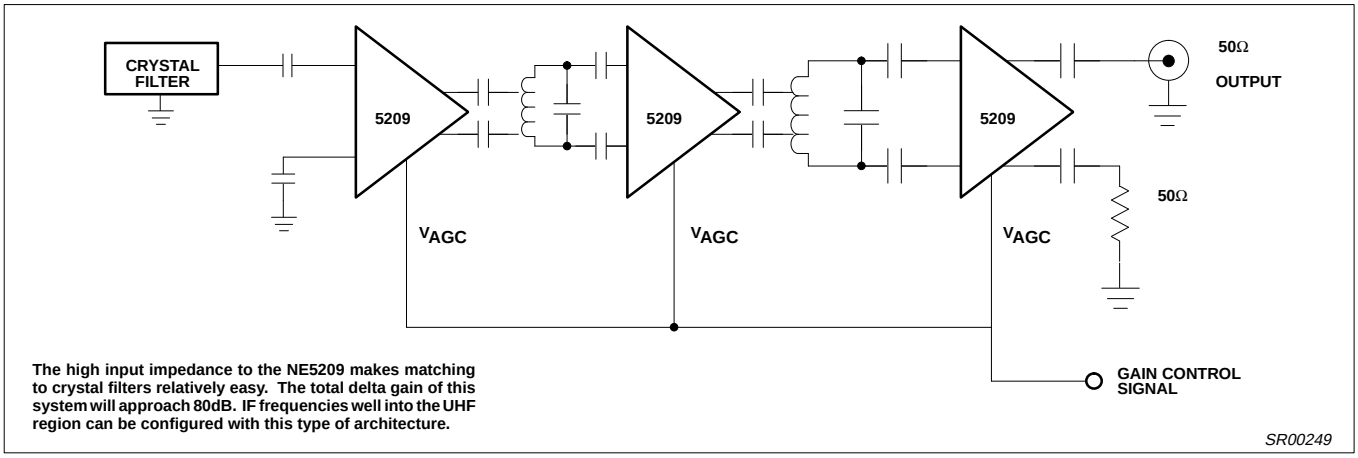


Figure 13. Receiver AGC IF Gain

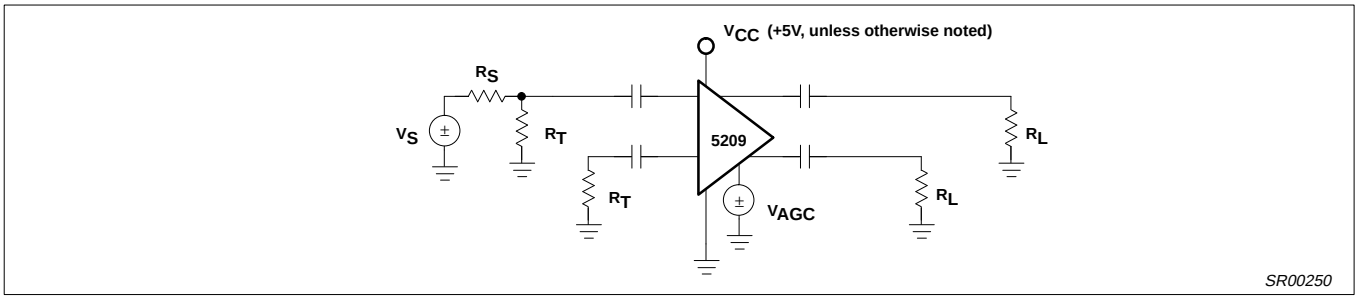


Figure 14. Test Set-up 1 (Used for all Graphs)

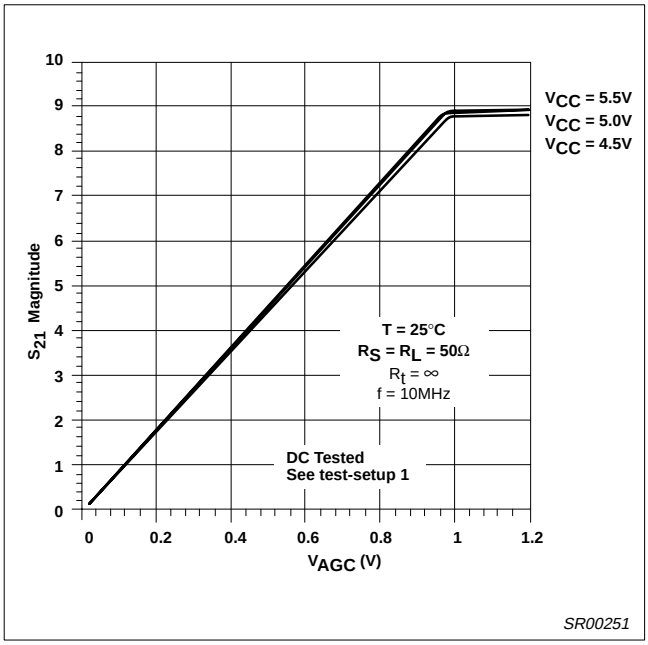


Figure 15. Gain vs V_{AGC} and V_{CC}

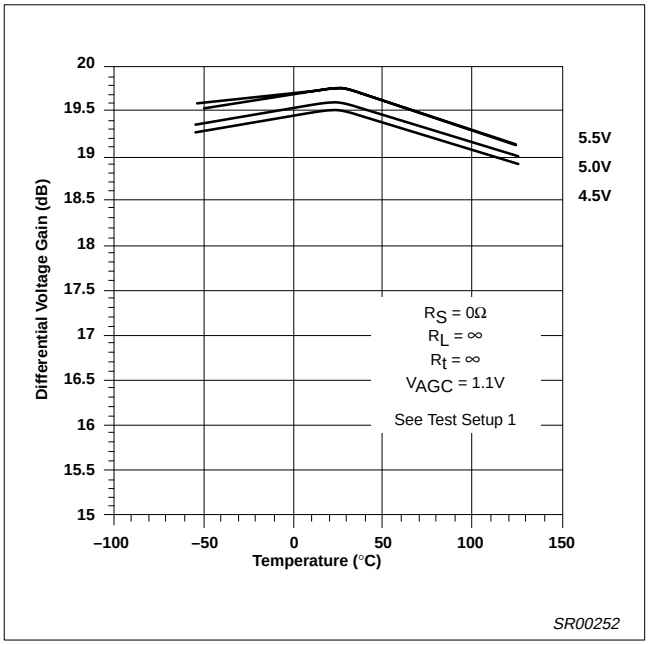


Figure 17. Voltage Gain vs Temperature and V_{CC}

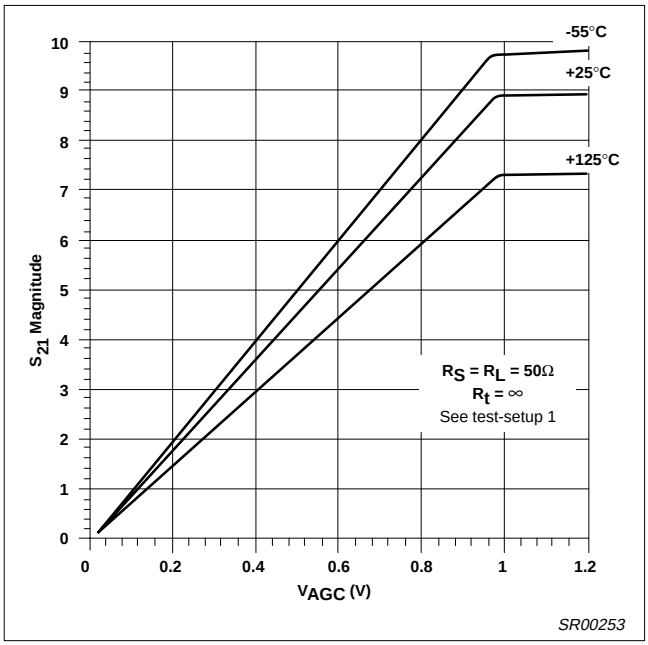


Figure 16. Insertion Gain vs V_{AGC} and Temperature

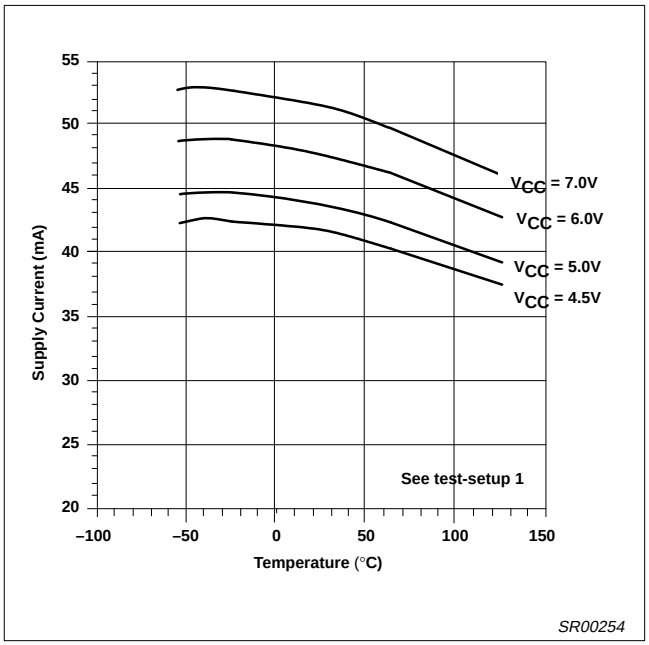


Figure 18. Supply Current vs Temperature and V_{CC}

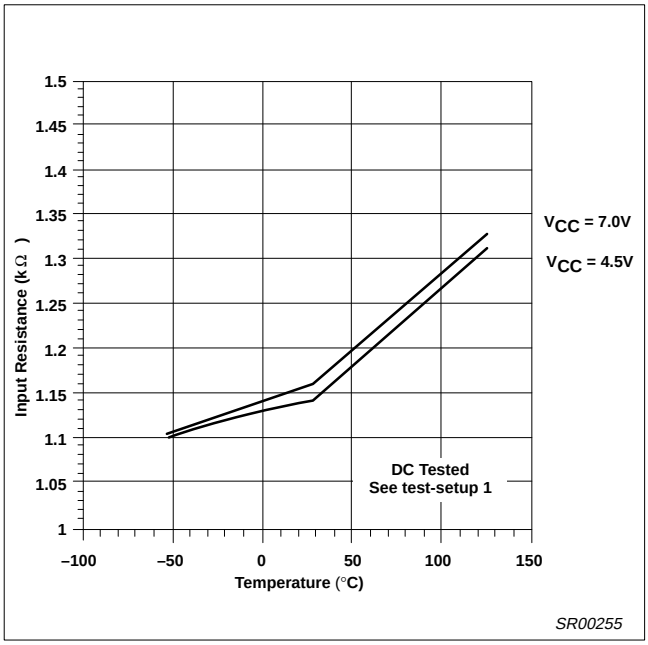


Figure 19. Input Resistance vs Temperature

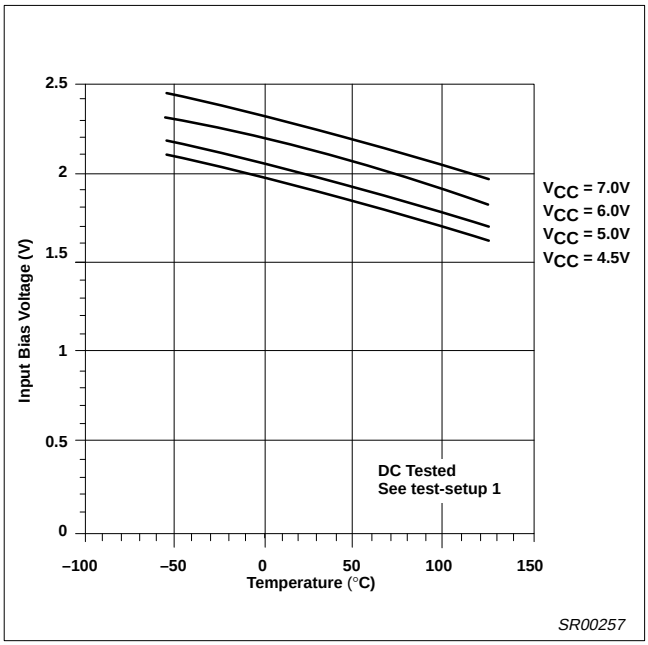


Figure 20. Input Bias Voltage vs Temperature

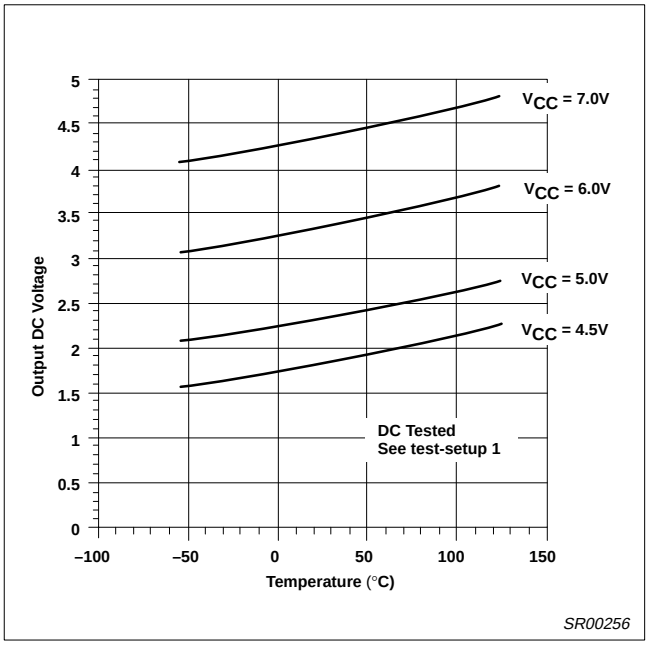


Figure 21. Output Bias Voltage vs Temperature and V_{CC}

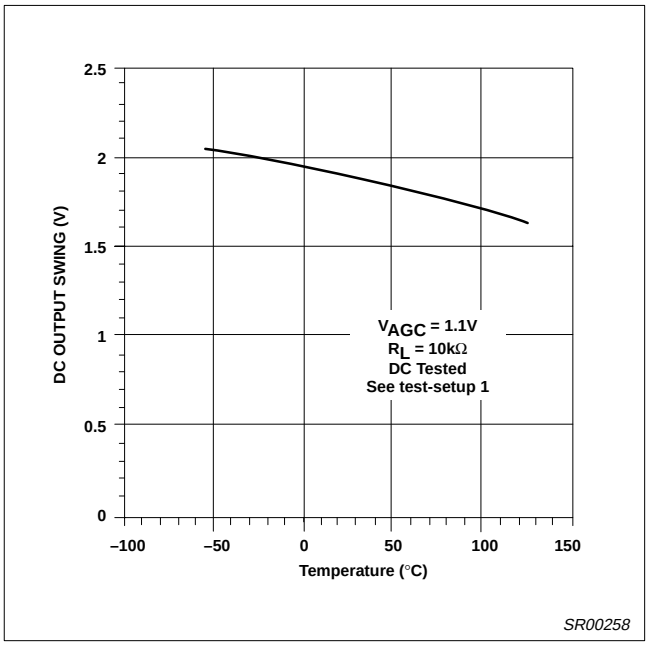


Figure 22. DC Output Swing vs Temperature

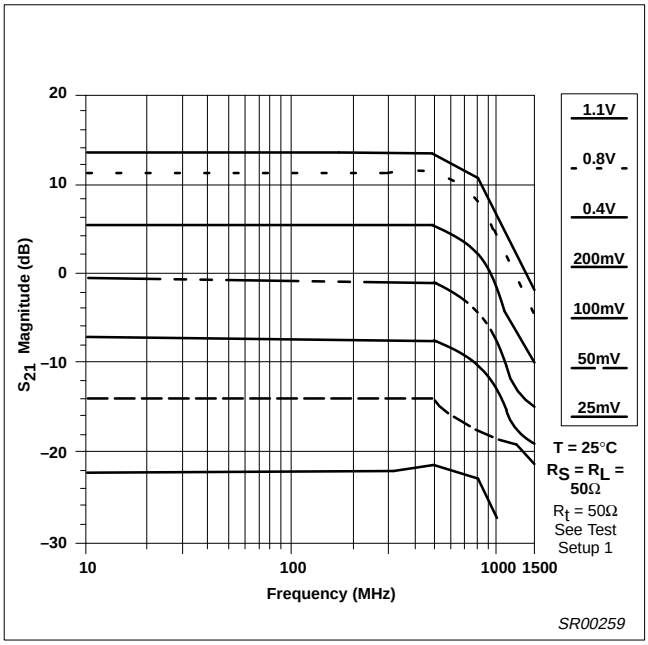


Figure 23. Insertion Gain vs Frequency and V_{AGC}

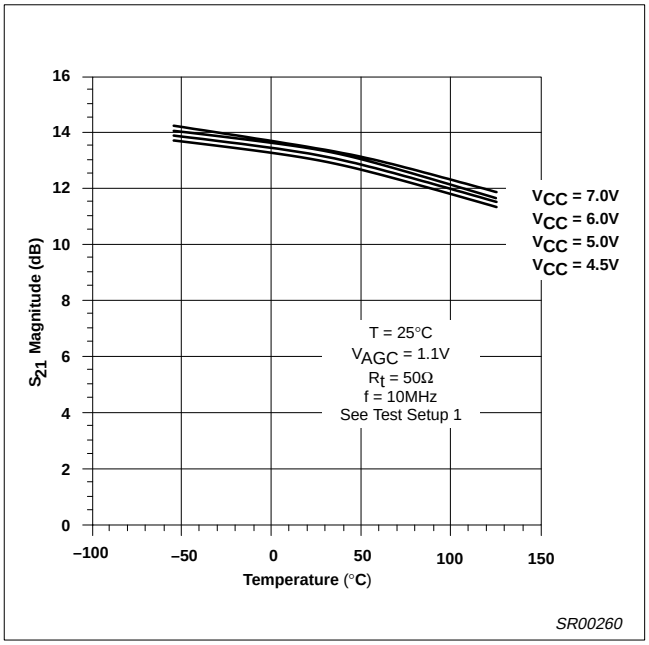


Figure 25. Insertion Gain vs Temperature and V_{CC}

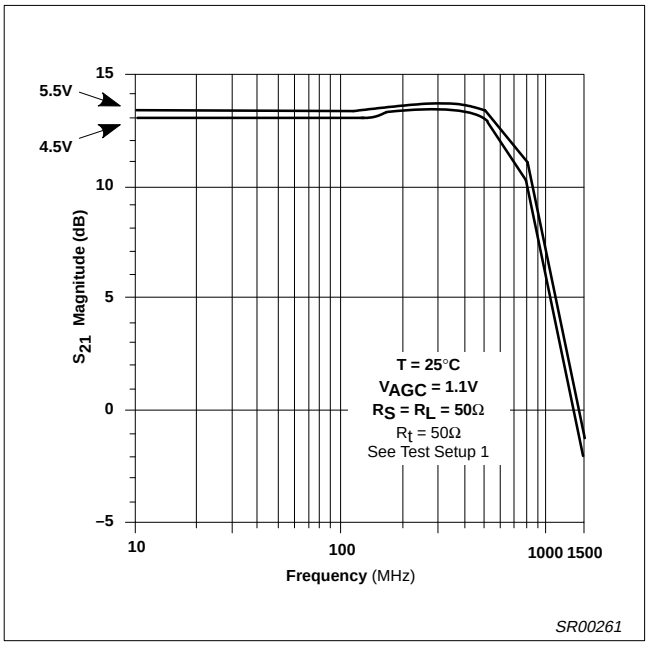


Figure 24. Insertion Gain vs Frequency and V_{CC}

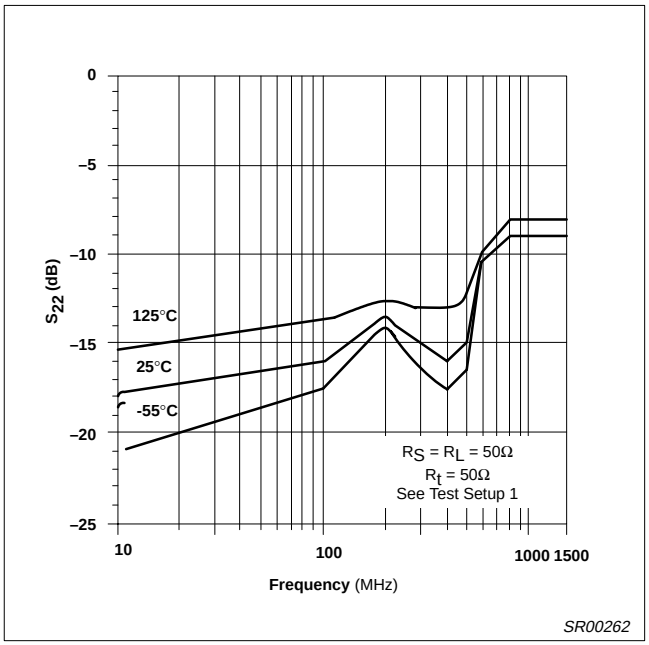


Figure 26. Output Return Loss vs Frequency

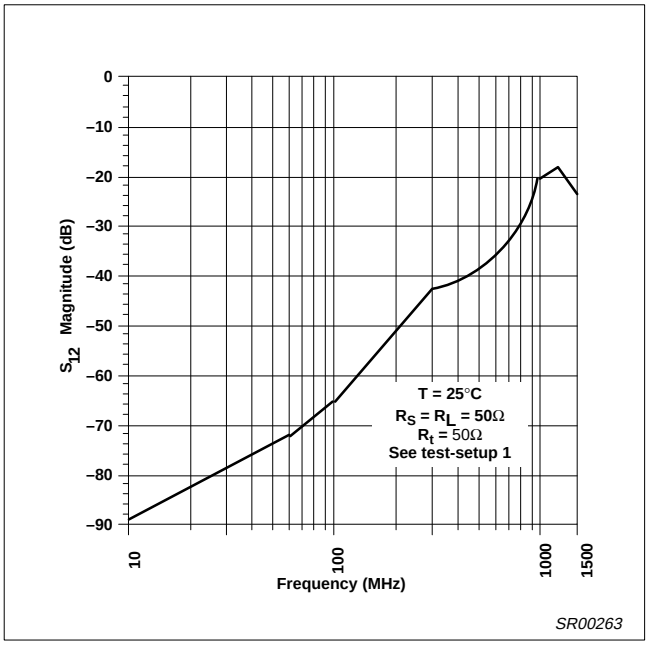


Figure 27. Reverse Isolation vs Frequency

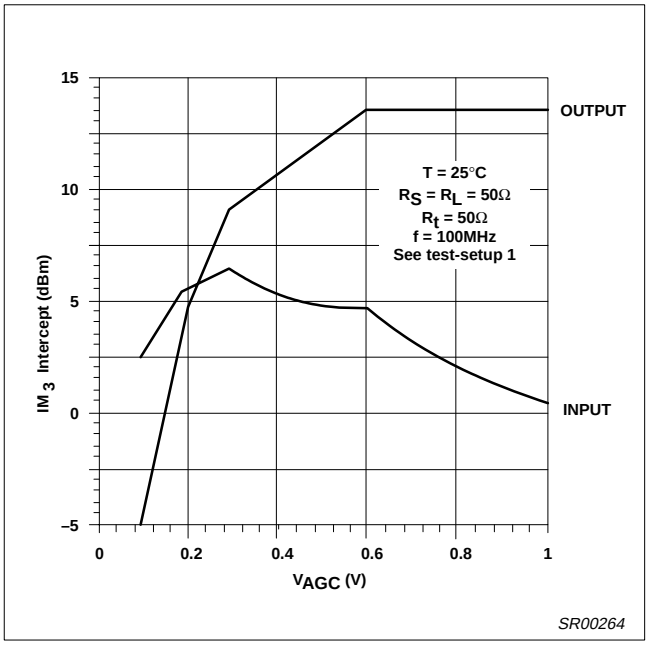


Figure 29. Third-Order Intermodulation Intercept vs V_{AGC}

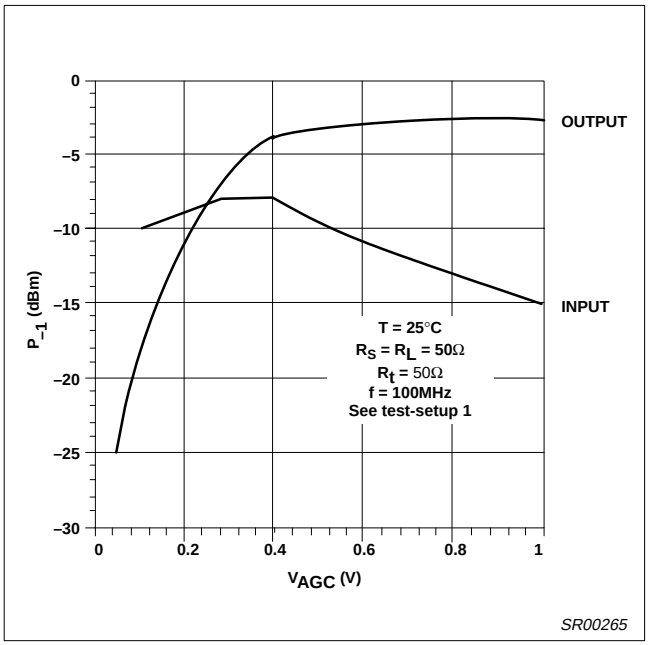


Figure 28. 1dB Gain Compression vs V_{AGC}

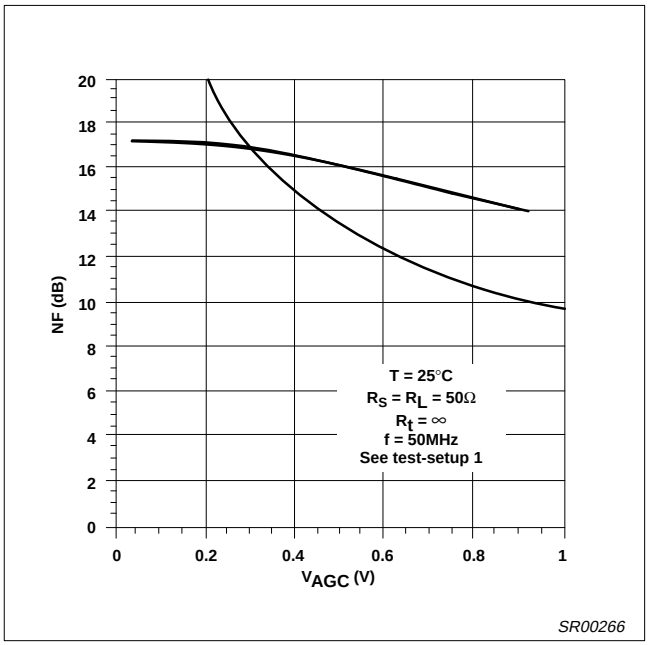


Figure 30. Noise Figure vs V_{AGC}

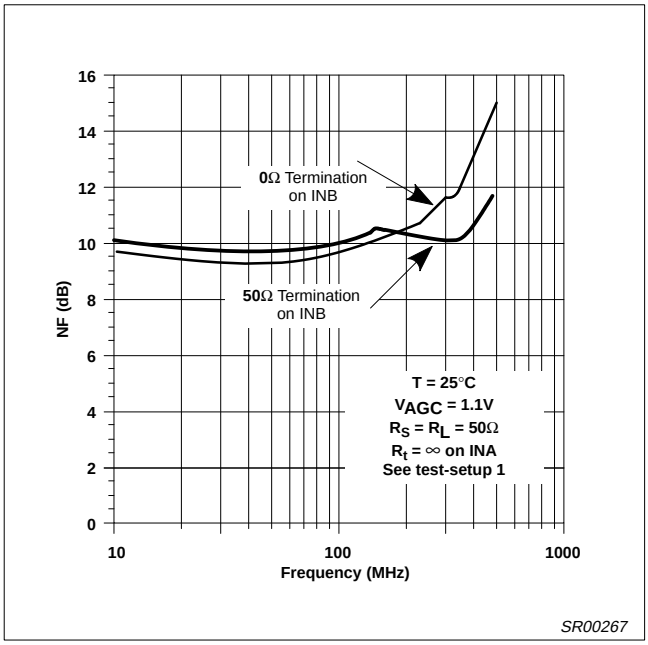


Figure 31. Noise Figure vs Frequency

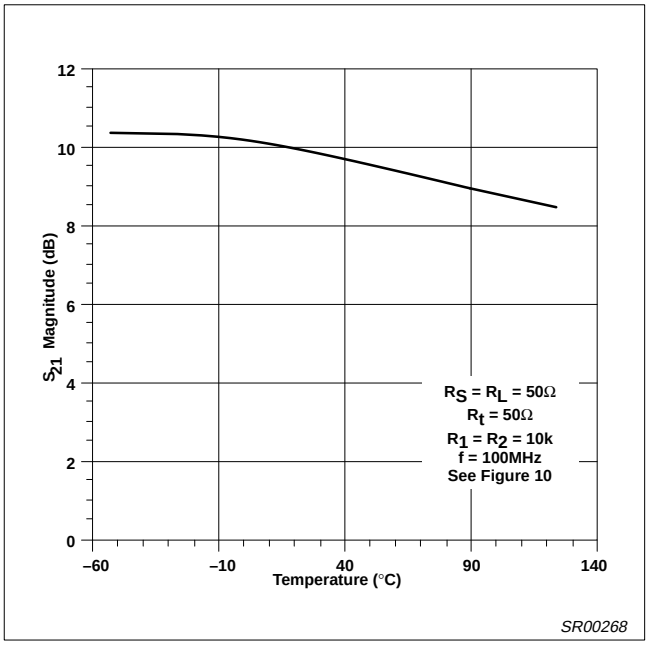


Figure 33. Fixed Gain vs Temperature

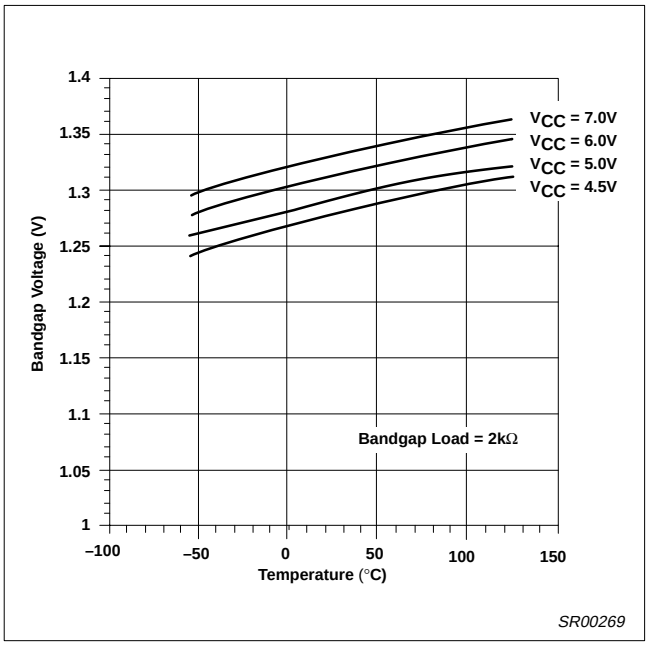


Figure 32. Bandgap Voltage vs Temperature and V_{CC}

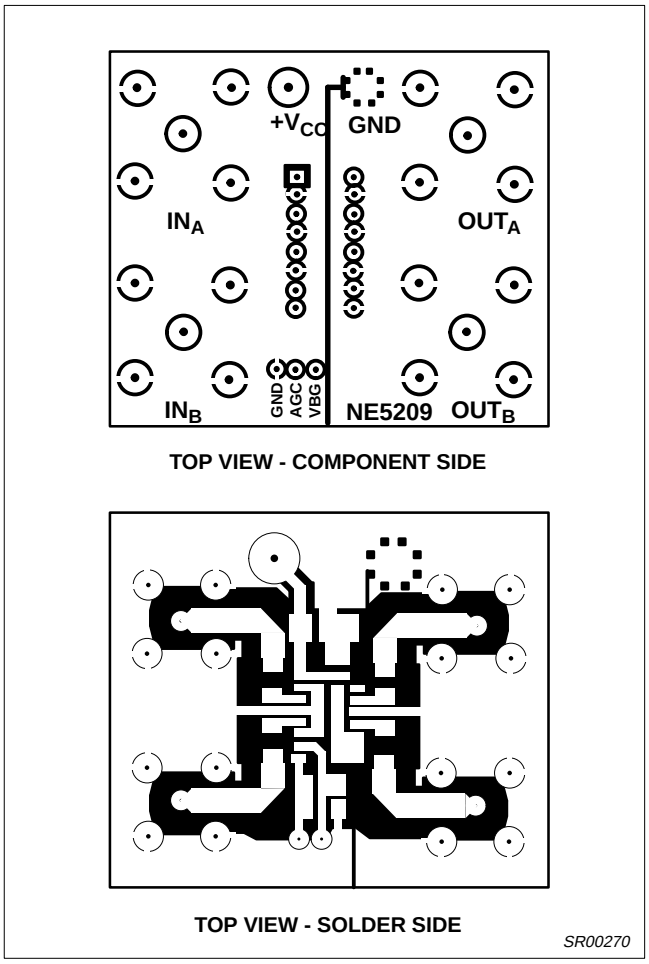
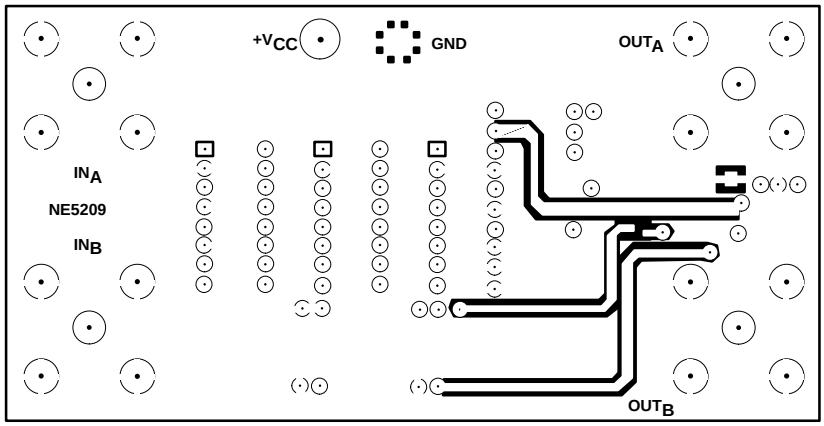
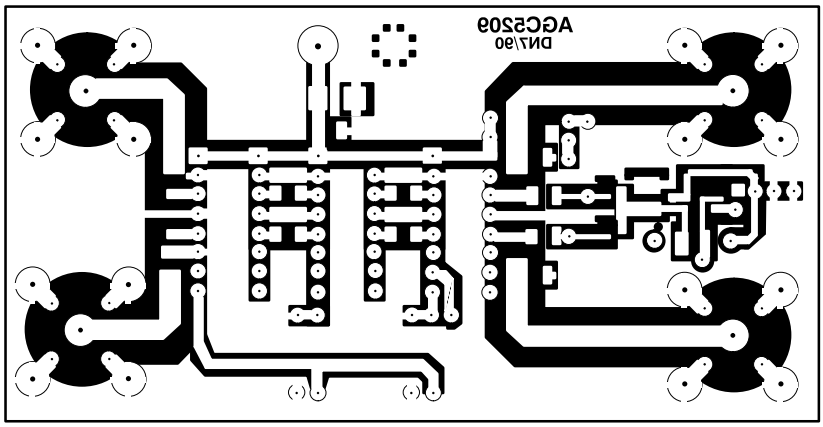


Figure 34. VGA AC Evaluation Board Layout



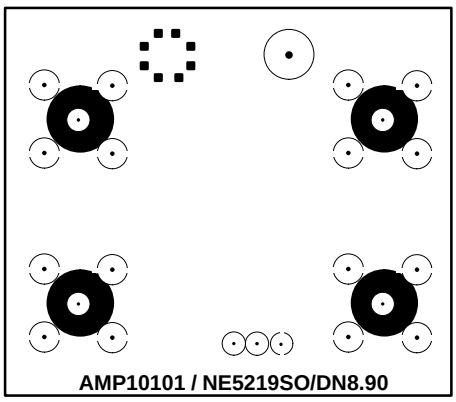
TOP VIEW - COMPONENT SIDE



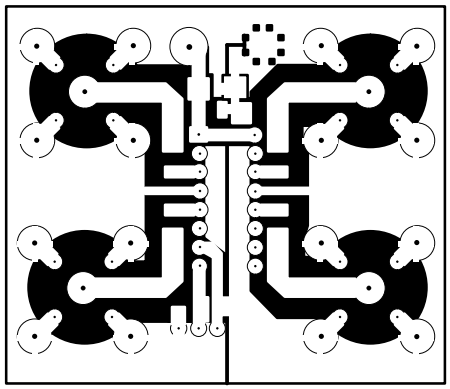
TOP VIEW - SOLDER SIDE

SR00271

Figure 35. AGC Configuration Using Cascaded NE5209s - Layout



TOP VIEW - COMPONENT SIDE



TOP VIEW - SOLDER SIDE

SR00272

Figure 36. VGA AC Evaluation Board Layout (DIP Package)

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Philips Semiconductors and Philips Electronics North America Corporation reserve the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

LIFE SUPPORT APPLICATIONS

Philips Semiconductors and Philips Electronics North America Corporation Products are not designed for use in life support appliances, devices, or systems where malfunction of a Philips Semiconductors and Philips Electronics North America Corporation Product can reasonably be expected to result in a personal injury. Philips Semiconductors and Philips Electronics North America Corporation customers using or selling Philips Semiconductors and Philips Electronics North America Corporation Products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors and Philips Electronics North America Corporation for any damages resulting from such improper use or sale.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

Philips Semiconductors and Philips Electronics North America Corporation register eligible circuits under the Semiconductor Chip Protection Act.
© Copyright Philips Electronics North America Corporation 1993
All rights reserved. Printed in U.S.A.